[0014] Figure 3 is a block diagram of a CBR rate controller in accordance with one embodiment of the present invention.

[0015] Figure 4 is a block diagram of a CBR bit allocator in accordance with one embodiment of the present invention.

[0016] Figure 5 is a block diagram of a dual CBR/VBR rate controller in accordance with one embodiment of the present invention.

[0017] Figure 6 is a block diagram of a core VBR rate controller in accordance with one embodiment of the present invention.

[0018] Figure 7 is a block diagram of an equivalent model of a VBR rate controller for one set of conditions.

[0019] Figure 8 is a plot illustrating exemplary quantizer step-size behavior for the dual VBR/CBR rate controller.

Like reference numerals refer to corresponding parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0020] Figure 2 is a block diagram of a video compression encoder 200 in accordance with one embodiment of the present invention. It will be understood that the video compression encoder is adapted to receive video images and encode the video images to generate an output bit stream in compliance with a block-based video compression standard such as MPEG-1, MPEG-2, MPEG-4, or H.264, etc.

[0021] Encoder 200 includes an MPEG motion estimation module 210, a macroblock coding decision module 220, a transform module 230 to perform a discrete cosine transform (DCT), a quantization module 240 to quantize the compressed DCT coefficients on a macroblock-per-macroblock basis according to a quantization step size, a variable length encode module 250 for encoding compressed image data into an output bitstream, and a programmable rate controller 260 for selecting the quantization step size. In one embodiment, quantization module 240 includes a virtual quantizer scale that takes on values from 2 to any arbitrarily high value, e.g., 512. An encoder video bitstream verification (VBV) buffer (not shown) may be included in the encoder. A VBV buffer is a model hypothetical decoder buffer used to determine potential decoder buffer underflow and overflow conditions. It is desirable that the bitstream remain VBV compliant such that a corresponding decoder does not suffer a deleterious underflow or overflow condition.